Atty. Docket No. PPW06-574DS
Serial No: 10/736,063

Remarks

Applicant and his representatives wish to thank Examiner Mitchell for the thorough examination of the present application and the clear explanations in the Office Action dated July 26, 2006. Claims 1, 16, and 17 have been amended. Claims 14 and 15 have been cancelled. New Claims 22 and 23 have been added. Therefore, Claims 1-12, and 16-23 are active in this application. No new matter is introduced by the present Amendment.

The present invention relates to a method of forming a gate in a semiconductor device comprising the steps of:

a) forming a shallow trench isolation (STI) to define an active region in a semiconductor substrate;

b) forming a gate oxide layer on the semiconductor substrate;

c) forming on the semiconductor substrate a sacrificial layer;

d) selectively etching the sacrificial layer to form a sidewall opening over the active region of the semiconductor substrate and the STI until the gate oxide is exposed;

e) forming a polycrystalline silicon layer on an area of the gate oxide layer exposed through the sidewall opening and on the sacrificial layer;

f) anisotropically etching the polycrystalline silicon layer such that sidewall gates remain on sidewalls of the sidewall opening, the sidewall gates having a minimum width; and

g) removing the sacrificial layer.

The cited references do not disclose or suggest, alone or taken together, a method comprising (i) etching sacrificial layer to form a sidewall opening over an active region of the semiconductor substrate and an STI until a gate oxide is exposed, and (ii) anisotropically etching a polycrystalline silicon layer deposited into the opening such that sidewall gates having a

minimum width remain on sidewalls of the sidewall opening (see steps d and f above). Thus, the present claims are patentable over the cited references.

The Rejection of Claims 1, 2, 5, 8, 11, 12, and 14-21 under 35 U.S.C. § 103(a)

The rejection of Claims 1, 2, 5, 8, 11, 12, and 14-21 under 35 U.S.C. § 103(a) as being unpatentable over Ahn (US 5,612,237) in combination with Rhodes (US 2004/0094784) is respectfully traversed.

Ahn discloses a method of manufacturing a flash EEPROM cell having a split-gate structure (col. 1, ll. 53-54). The method comprises forming an oxide film by means of the oxidation process using nitride film patterned by the etching process as an oxidation prevention layer such as the LOCOS (Local Oxidation of Silicon) process such that a so called bird's beak (BB) is created on both sides of the oxide film and removing the exposed portion of the oxide film by means of the etching process using the patterned nitride film as the etching mask, thereby exposing a portion of the silicon substrate and forming first and second residual oxide films having a symmetric structure with the bird's beak (BB) portion in the oxide film being left (col. 3, ll. 4-17). Subsequently, a tunnel oxide film is formed on the exposed silicon substrate (col. 3, ll. 20-21). The first and second floating gates are formed on the etching surfaces of the patterned nitride film and the first and second residual oxide films in spacer form (col. 3, ll. 28-33). The drain region and the first and second source regions are formed by means of the self-aligned ion implantation method using the first and second floating gates and the first and second residual oxide films (col. 3, ll. 39-44).

Thus assuming for the sake of argument that the tunnel oxide 25 of Ahn corresponds to the presently claimed gate oxide, because Ahn does not form gate oxide until after the LOCOS oxide is etched, Ahn cannot etch the sacrificial layer over a LOCOS oxide until the gate oxide is exposed. Therefore, Ahn is deficient with respect to a method comprising (i) etching sacrificial layer to form a sidewall opening over an active region of the semiconductor substrate and an STI until a gate oxide is exposed, and (ii) anisotropically etching a polycrystalline silicon layer

deposited into the opening such that sidewall gates having a minimum width remain on sidewalls of the sidewall opening, as recited in Claim 1.

It is believed that Ahn uses the LOCOS process to form bird's beaks. It is further believed that Ahn may need the bird's beaks in order to form the first and second residual oxide films. Subsequently, it is believed that Ahn may use the first and second residual oxide films in spacer form to form the first and second floating gates. Finally, it is believed that Ahn uses the first and second floating gates and the first and second residual oxide films to form the drain region. As a result, it does not seem possible for Ahn to form an opening over both an isolation structure and an active region.

Rhodes discloses a barrier implanted region of a first conductivity type located below an isolation region of a pixel sensor cell and spaced from a doped region of a second conductivity type of a photodiode of the pixel sensor cell (Abstract, ll. 1-4). Rhodes appears silent as to a method comprising (i) etching a sacrificial layer to form a sidewall opening over an active region of the semiconductor substrate and an STI until a gate oxide is exposed, and (ii) anisotropically etching a polycrystalline silicon layer deposited into the opening such that sidewall gates having a minimum width remain on sidewalls of the sidewall opening. Therefore, Rhodes fails to cure all of the deficiencies of Ahn.

Consequently, no possible combination of Ahn and Rhodes, can suggest a method comprising (i) etching sacrificial layer to form a sidewall opening over an active region of the semiconductor substrate and an STI until a gate oxide is exposed, and (ii) anisotropically etching a polycrystalline silicon layer deposited into the opening such that sidewall gates having a minimum width remain on sidewalls of the sidewall opening. Therefore, this ground of rejection is unsustainable, and should be withdrawn.

Claims 2, 5, 8, 11, 12, 14, and 16-21 depend from Claim 1, and thus include all of the limitations of Claim 1. Therefore, Claims 2, 5, 8, 11, 12, 14, and 16-21 are patentable over Ahn and Rhodes for essentially the same reasons as Claim 1.

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The Rejection of Claims 3, 4, 9, and 10 under 35 U.S.C. § 103(a)

The rejection of Claims 3, 4, 9, and 10 under 35 U.S.C. § 103(a) as being unpatentable over Ahn (US 5,612,237) and Rhodes (US 2004/0094784) and in further combination with Kim et al. (US 2002/0001935, hereinafter "Kim") is respectfully traversed.

As explained above, the combination of Ahn and Rhodes is saliently deficient with respect to a method comprising (i) etching sacrificial layer to form a sidewall opening over an active region of the semiconductor substrate and an STI until a gate oxide is exposed, and (ii) anisotropically etching a polycrystalline silicon layer deposited into the opening such that sidewall gates having a minimum width remain on sidewalls of the sidewall opening, as recited in Claim 1.

Kim discloses a method of forming a gate electrode in semiconductor device which can prevent transformation of the gate electrode (Abstract, ll. 1-3). Kim appears silent as to a method comprising (i) etching sacrificial layer to form a sidewall opening over an active region of the semiconductor substrate and an STI until a gate oxide is exposed, and (ii) anisotropically etching a polycrystalline silicon layer deposited into the opening such that sidewall gates having a minimum width remain on sidewalls of the sidewall opening. Therefore, Kim fails to cure the deficiencies of the combination of Ahn and Rhodes.

Consequently, no possible combination of Ahn, Rhodes, and Kim, can suggest a method comprising (i) etching sacrificial layer to form a sidewall opening over an active region of the semiconductor substrate and an STI until a gate oxide is exposed, and (ii) anisotropically etching a polycrystalline silicon layer deposited into the opening such that sidewall gates having a minimum width remain on sidewalls of the sidewall opening. Therefore, this ground of rejection is unsustainable, and should be withdrawn.

Claims 3, 4, 9, and 10 depend from Claim 1, and thus include all of the limitations of Claim 1. Therefore, Claims 3, 4, 9, and 10 are patentable over Ahn, Rhodes, in further combination with Kim for essentially the same reasons as Claim 1.

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Conclusions

In view of the above amendments and remarks, all bases for objection and rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,

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